

## CLAIMS

Please amend the following claims.

*Sub C1*  
*B1*

1. (Twice Amended) A field effect transistor, comprising:  
a substrate having a recess in a surface thereof, the recess having a bottom portion and substantially vertical sidewalls;  
a gate dielectric layer disposed superjacent the bottom portion of the recess and adjacent the substantially vertical sidewalls;  
a gate electrode overlying the gate dielectric layer; and source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls, said gate electrode extending to a less shallow depth within said substrate than a depth at which the source/drain terminals are disposed; wherein the source/drain terminals comprise an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess.

*sub C3*  
*B2*

4. (Twice Amended) A field effect transistor, comprising:  
a substrate having a recess in a surface thereof, the recess having bottom portion and tapered sidewalls, the tapered sidewall surfaces forming an obtuse angle with respect to the bottom portions of the recess;  
a gate dielectric layer disposed superjacent the bottom portion of the recess and adjacent the tapered sidewalls;  
a gate electrode overlying the gate dielectric layer; and source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls;  
wherein the source/drain terminals comprise an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess.

sub C5

7. (Twice Amended) A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having a curvilinear

shape;

a gate dielectric layer disposed superjacent the curvilinear recess;

B3 a gate electrode overlying the gate dielectric layer; and source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls;

wherein the source/drain terminals comprise an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the curvilinear sides of the recess.